Upset Manifestations in Embedded Digital Signal Processors due to Single Event Effects

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Abstract– Digital Signal Processors (DSP) embedded in FPGAs are irradiated with heavy ions in order to further understand the impact of particle-induced Single Event Effects (SEE) to their functionality. SEE upset duration and start-time measurements taken of various DSPs simultaneously during irradiation experiments provide a portrait of the various contributing upset mechanism as well as on-orbit rate estimates.

I. Introduction

DIGITAL Signal Processors (DSP) are devices that provide high-speed arithmetic computational capability to digital systems. They are available in standalone devices or can be found embedded in micro-processors and Field Programmable Gate Arrays (FPGA), and can be built into Application Specific Integrated Circuits (ASICs). The DSPs available in re-configurable FPGAs are especially useful to applications that are only realized by the capability of reprogrammable algorithms, such as the implementation of ever-changing imaging and communication standards. The massive parallel capability offered by the nature of the FPGA architecture, also allows for considerable computational bandwidth while operating at moderate frequencies. FPGA DSP applications include routers, modems, signal converters and modulators, and image compressors, just to name a few. DSPs are the essential elements in the design of modern communications systems and processors.

The capability provided by FPGA-based DSP systems is also being sought after by space system developers for commercial, scientific and military applications. Heavy ion SEE test campaigns have been carried out for RAM-based FPGA [1] and anti-fuse-based FPGA DSPs [2][3], in order to understand the actual response of the devices in the charged particle environment of space. The SEE results that have been introduced to the community demonstrate that the impact of SEUs in DSPs strongly depend on the type of computation being carried out by the DSPs, resulting in either transitory or persistent effects [1], and on the operating frequency [3].

In this work, SEE testing was carried out on DSPs in FPGAs employing radiation hardened RAM-based FPGA technologies. The results are further analyzed and serve to differentiate between the main sources and mechanisms of the errors measured, and the impact of each. The measurements of static and dynamic cross-sections provide on-orbit performance rates, while time duration of individual SEUs on single and multiple DSPs supply additional understanding on the source mechanisms that contribute to the overall upset sensitivity of the DSPs in a FPGA design. Motivating this detailed visibility instrumented into these tests is the need to provide critical information for assisting high reliability and space designers and system engineers in making wise design trades and design mitigation choices.

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II. Technical Background

A. Digital Signal Processors in Virtex FPGAs

The DSP cells studied in this work are the ones found in the space-grade Xilinx Virtex-4 and Virtex-5 RAM-based FPGAs, which provided hundreds of DSP cells to the FPGA designer, each with the capability for several 48-bit wide input operators and a 48-bit output operand. The Xilinx Virtex-4 is based on 90-nm CMOS technology, while the Virtex-5 FPGA is 65-nm. A summary of the key differences between the Virtex-4 and 5 FPGAs with respect to this work are listed in Table I.

Table I. DSPs in the Virtex-4 vs. Virtex-5.

	Virtex-4 V4QV-SX55	Virtex-5 V5QV-FX130T
RHBD Config. System	No	Yes
RHBD CLBs	No	Yes
No. of CLB flip-flops	49,152	81,920
RHBD DSPs	No	No
DSP Cell Architecture	DSP48	DSP48E
No. of DSPs	512	320
Arrangement	64 DSPs in 8 col.	80 DSPs in 4 col.

The Virtex-5 FPGAs employ a radiation hardened-by design (RHBD) technology which provides the user with upset-hardened configuration cells, a triplicated FPGA configuration engine, and configuration logic blocks (CLBs); including optional Single Event Transient (SET) filters at the upset-hardened CLB flip-flop's clock, data and control inputs. The Virtex-4 FPGA on the other hand, employs a non-hardened technology. Fig. 1 shows a block diagram of the Virtex-5 DSP, illustrating the basic mechanisms that make up the DSP48E cell. The DSP cells in the Virtex-4 and Virtex-5 FPGAs consist fundamentally of a multiplier and an addition/subtraction element, with a user-controlled multiplexer in between them. The Virtex DSPs contain a rich set of configurable registers; these are the input operator registers, which are the A1, A2, B1, B2 and C registers, the intermediate multiplier stage register M, as well as the output

operand register P; these registers allow for the high operating frequency capability of the Virtex DSPs. In both FPGAs, the user can dynamically select the type of operation executed and which operator of the DSP is used by controlling the operational mode of the selection multiplexers.

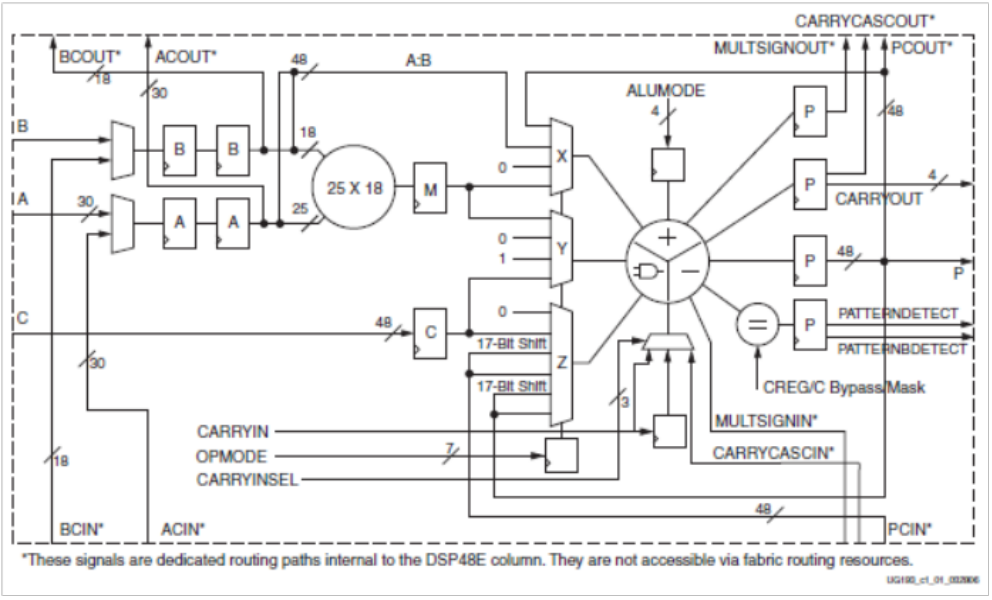

Fig. 1. Virtex-5 DSP48E Cell.

The enhanced Virtex-5 DSP cell has some features not available in the Virtex-4 DSP cell, including a dedicated C input operator register, a 48-bit Arithmetic Logic Unit (ALU), and pattern detection capability. Furthermore, the DSP48E can be split into 24-bit dual or 12-bit quad Single-Instruction Multiple Data (SIMD) operation, effectively multiplying the available DSP slices in the FPGA.

B. Single Event Effect Susceptibility

FPGA designs implemented in RAM-based FPGAs are susceptible to suffering radiation induced upsets that can affect both, the *configuration plane*, which defines the FPGA design implemented, or the *functional plane*, defined by the actual micro-circuits that make up the FPGA designs functionality. The configuration plane sensitivity is not an issue for ASICs or antifuse-based FPGAs, where the digital functions are permanently hard-coded into the device and are not subject to upsets, only hard fails. In general, the SEE source mechanisms that cause these upsets are due to either Single Event Transient (SET) pulses or direct Single Event Upsets (SEU); always resulting in a change of state of any of the digital storage elements that makes up the design [4].

In a FPGA design's functional plane, upsets can occur in the CLB flip-flops, I/O registers, embedded memory cells, or any other embedded storage elements of the FPGA, which include internal structures like half-latches [5], and user structures like the DSPs, block RAMs [6], or multi-gigabit transceivers (MGT) [7]. SEEs induced by the elements that make up the design's configuration plane, actually distort the design's implementation, potentially corrupting the designs functionally until corrected. Also contributing to the sensitivity of the configuration plane is the upset susceptibility of the configuration engine controller. Regardless of whether the upset is sourced at the configuration or functional plane, the actual impact on the design's functionality can be various, from simple glitch-like momentary errors in the function, or non-persistent SEUs, to persistent errors, where the function becomes inaccessible until the appropriate recovery mechanisms are actuated. Events that result in persistent functionality errors are referred to as Single Event Functional Interrupts (SEFIs).

The upsets to a design's synchronous or storage elements that are due to SETs, occur when the binary state of the element becomes corrupt by an inadvertent latching of the SET pulse on either the data or control inputs, or corrupted by an actual SET in the clock input of the element. The susceptibility to corruption by SETs has been shown to be heavily influenced by the operating frequency [3]. Even though the source of the transients can be numerous, all the resulting effects on a design can be bounded by the direct upset effects, or *static effects*, and *dynamic effects*, which include all the effects from SETs as well as direct upsets.

Much work has been carried out in characterizing the upset susceptibility of the configuration planes of the RAM-based FPGAs Virtex-4 [8], [9] and Virtex- 5 [10]. Beam-proven mitigation techniques for configuration plane upsets are available [11][12][13]. These make use of the partial-reconfiguration capability of the device, allowing non-intrusive scrubbing of configuration upsets. Different types of scrubbing mitigation approaches have been studied and demonstrated, with various levels of sophistication, ranging from simpler "blind" scrubbing techniques, all the way to "surgical" scrubbing that makes use of configuration image

masks and external memory, to pin-point and reproduce particular bits of the configuration image's bit-stream. Each approach results in a FPGA system with different levels of susceptibility, requiring careful scrutiny during selection [13][14].

The DSP elements found in FPGAs are essentially arithmetic blocks that contain synchronous elements, logic elements and dedicated internal routing. Thus the functional response of a DSP cell to SEEs is not expected to be unlike any other configurable element of an FPGA, with a configuration plane and functional plane sensitivity, and distinct dynamic and static sensitivity profiles, as it's been shown [1][3]. The wide selection of arithmetic operations available to the user are one of the reasons DSP elements are so attractive to designers, but for SEE characterization, this wide selection results in a large test matrix that makes characterization of all possible operations unrealistic. For this reason, the SEE characterization of FPGA-based DSPs has been limited to operations involving the basic DSP arithmetic functions, which are addition/subtraction, multiplication, and accumulative operations. By using these three basic operations, the fundamental aspects of the DSPs are exercised during the testing, including the addition/subtraction unit, the multiplier unit and the feedback path. The sensitivity of all DSP applications can be analyzed by these three basic operations. This DSP characterization approach was first presented in [1] for RAM-based FPGAs, and was also employed in [2] for fuse-based FPGAs.

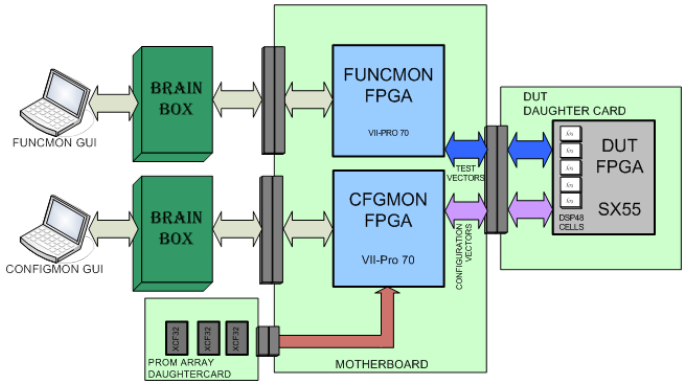

Fig. 2. XRTC SEE Test Setup, shown for Virtex-4 SX-55 FPGA DUT.

III. Test Setup and Experiments

The experimental campaigns were carried out with the test hardware developed by the Xilinx Radiation Test Consortium (XRTC), using heavy-ion beams in air at the Texas A&M cyclotron and in vacuum at the Lawrence-Berkeley National Laboratory cyclotron, over the course of 2008 through 2010, with SEE test reports available [15]. The XRTC hardware platform provides a direct interface for real-time functional verification and configuration management in parallel, since two dedicated FPGAs are used to interface to the FPGA under test (DUT). The XRTC hardware setup is illustrated in Fig. 2. In the setup, one FPGA is completely dedicated to monitor the DUTs functional status (FuncMon), while the second FPGA monitors the configuration system (ConfigMon) through the parallel SMAP configuration port of the DUT FPGA. The test user has two separate interfaces to the ConfigMon and FuncMon FPGAs.

Two main types of experiments were developed, a static test and a dynamic test. The goal of the static test was to obtain the static cross-sections of the internal user registers of each DSP cell, (P, M, C, A and B), which can be located in Fig. 1. For the static tests, all of the DSP cells available in the DUT FPGA were connected to global operators and controls, and each of the outputs of all the DSP cells were multiplexed into a single 48-bit vector. All control and input operators to the static DSP structures and the output multiplexer were also provided by the FuncMon FPGA. The output of the multiplexer was captured for each of the DSP cells and for each DSP register type after each irradiation period.

The dynamic test consisted of executing each of the three basic fundamental operations of the DSP while verifying the output of the cells being irradiated. Upon detection of an erroneous sample, an error flag is activated, latching the test timers and initiating duration counters. This error flag was maintained until four continuous valid samples are detected by the verification system. This provides a "clutch-like" mechanism in order to deem that the event has truly ended. Thus for each SEU detected, data was captured with the duration of each upset manifestation, as well as the exact time when the error occurred, allowing visibility into simultaneous effects across the DSP cells in the DUT FPGA.

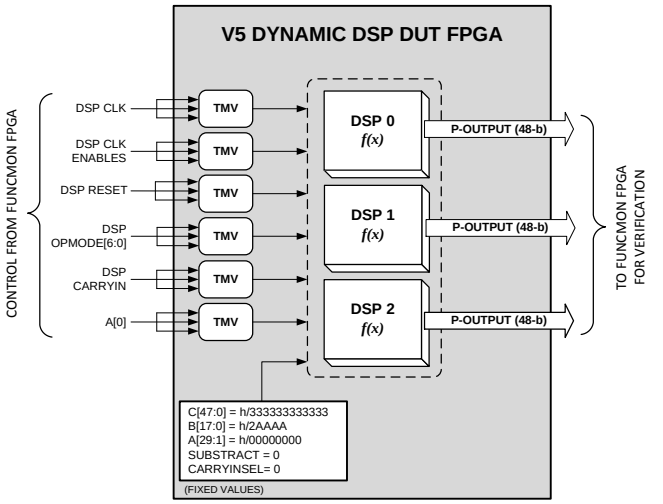

Fig. 3. DSP Dynamic Test Design Block Diagram.

For the dynamic tests, triple-majority redundant (TMR) DSP cells with voted outputs and a shared clock tree were developed, along with conventional single-string DSP cell arrangements. An illustration of the dynamic DUT design block diagram is illustrated in Fig. 3, where it is shown how all three of the test structures share controls, clock enables, clock and reset. To eliminate the possibility of I/O corruption affecting the test, all control inputs are triplicated and voted asynchronously. Due to the large number of I/O required to track every bit of the DSP outputs, the input operators A, B and C were held to fixed values, with exception of the A[0] bit, which was used to provide an alternating pattern input

operator for the multiplication tests. For the addition tests the OpMode was switched every clock cycle to alternate between the addition operations [A:B + 1] and [C + 1]. For the accumulation tests, the DSPs were setup to add one to the P-register value every clock cycle, effectively creating a 48-bit counter.

During all experiments, static and dynamic, the DUT FPGA design's configuration image was continuously read-back and scrubbed to correct for any configuration plane errors, and continuously monitored for configuration engine upsets. If a configuration engine upset or Single Event Effect Functional Interrupt (SEFI) was detected, the DUT FPGA was reconfigured. For the dynamic tests, the DUT was exercised at three different frequencies, 6.25, 12.5 and 25MHz.

IV. Results

A. Static and Dynamic Results

Static and dynamic cross-sections vs. Linear Energy Transfer (LET) from heavy-ions were obtained for the DSP registers and for the three basic operations. On-orbit upset rates were calculated using CRÈME-MC[16], employing an effective sensitive volume with dimensions defined by the limiting or saturated cross-section of each type of SEE measurement. The orbit used for the upset rate calculation is a geosynchronous orbit (36,000 km), with 0.15 in. of Aluminum shielding. Static results demonstrate that the M multiplier register possesses a higher per bit sensitivity than the other registers, affecting the overall register upset rate, as is shown in the cross-section plots of Fig. 4, where the M bits clearly standout.

Table II. DSP48E Register Static Upset Rates.

DSP48E Register	Register Upset Rate (/day)	Bit Upset Rate (/day)
A (30-bit)	$1.00\text{x}10^{-5}$	$3.20\text{x}10^{-7}$
B (18-bit)	$1.23\text{x}10^{-5}$	$3.20\text{x}10^{-7}$
C (48-bit)	$1.73\text{x}10^{-5}$	$3.20\text{x}10^{-7}$
M (36-bit)	$3.52\text{x}10^{-5}$	$1.83\text{x}10^{-6}$
P (48-bit)	$1.73\text{x}10^{-5}$	$3.20\text{x}10^{-7}$

Table III. Dynamic and Static Rates of DSP48E basic operations in GEO

Operation	Dynamic Upset Rate (/day)	Static Upset Rate (/day)	Static Contribution
Addition	$1.57\text{x}10^{-4}$	$5.05\text{x}10^{-4}$	32%
Multiplication	$1.82\text{x}10^{-4}$	$1.01\text{x}10^{-4}$	56%
Accumulation	$3.78\text{x}10^{-5}$	$1.73\text{x}10^{-5}$	45%

The resulting static cross-sections result in the upset rates listed in Table II for geosynchronous orbit. Table III shows the upset rates for the dynamic operations, with the percentage of each dynamic upset rate that is due to the static effects shown on the right-most column. To compute this static contribution percentage, the rate of each register employed by the particular dynamic operation has to be summed. For example, since the accumulation operation tests only employed the P-Register, the static upset contribution of the accumulation dynamic test is the static upset rate of the P-Register, which is $1.73\text{x}10^{-5}$ upsets per day.

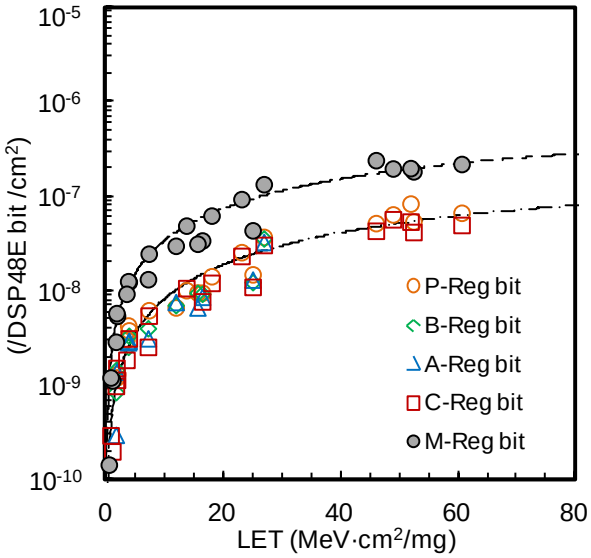

Fig. 4. Static Cross-Sections for DSP48E Register.

B. SEU Duration Measurements

The dynamic tests allowed for measurements to be taken of the duration of each upset event suffered by the DSPs. The distribution of event durations is shown in the four plots of Fig. 10. In these plots, each event is represented with a circle, and they are ordered by occurrence, from left to right, within each run, and then each run is ordered by the LET used also from left to right. These plots show every event observed during the testing, including configuration engine SEFI events, which resulted in SEU durations lasting the re-configuration time of the device. In Fig. 10 (a) and (b), the color scale variations illustrate the different LETs utilized; ranging from 2.0 (blue), to 15.0 (yellow and orange), and 38.0 MeV·mg/cm^2 (burgundy). And in Fig. 10 (c) and (d), the split between LETs and events is shown by a dashed vertical line, with the LETs being 1.6, 2.4, 7.3 and 25 MeV·mg/cm^2.

Three main time regimes can be extracted from the event duration distribution (*T-duration*) and repeatability; 1) a duration from 50 micro-seconds to the duration of the scrub and configuration cycle, which is approx. 250 milliseconds for the Virtex-4 and 400 milliseconds for the Virtex-5; 2) a duration of a single clock cycle, lasting for the duration of the test frequency clock period; and 3), a duration of greater than one clock-cycle to approximately 50 microseconds. A fourth, less obvious, regime can be inferred- events that last longer than the scrub-cycle or device re-configuration time.

1) T-duration > 50 microseconds to T-duration ≈ Time of Device Scrub/Reconfiguration Cycle

These events, which have a random duration distribution within the regime, are attributed to SEUs in the configuration plane of the device. As stated, the DUT design was continuously being scrubbed during the irradiation by the configuration monitoring system, thus when a configuration upset took place that affected the design, it would only be corrected upon the next scrub cycle, which was asynchronous

to when the upset occurred, thus resulting in a random time duration measurement. Some events lasted longer since they must have occurred during the read-back cycle or right after that particular bit was scrubbed, requiring a full read-back and scrub cycle to occur before being corrected. In general, the maximum time of these events would always be the full scrub cycle time. It can be seen that these events are drastically more numerous for the Virtex-4 device than for the Virtex-5 device, demonstrating the effectiveness of the Virtex-5 Rad-Hard-by-Design (RHBD) configuration cells. An as is shown in Fig. 10, the Virtex-4 device suffered so many configuration upsets during the testing, that repeatable duration events from the functional plane were not captured nearly as often as for the Virtex-5, where configuration upsets were not observed until LETs greater than 15 MeV·cm^2/mg were achieved. Discriminating these events from the measurement pool, cross-sections for configuration events affecting the DSPs can be extracted, and these are shown in Fig. 5.

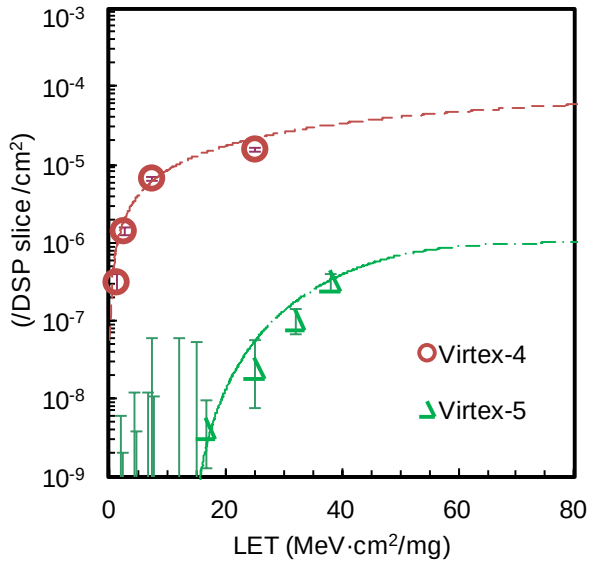

Fig. 5. DSP cell configuration upsets for the Virtex-4 and Virtex-5 DUT designs.

2) T-duration = Clock-Cycle Duration Events

The events in this regime last the period of the test frequencies utilized, and are the expected SEU manifestations of the DSP functional plane. The frequency used in the Virtex-4 tests was only at 25MHz, or 40 nanoseconds, and for the Virtex-5 was at 6.25, 12.5 and 25MHz. The majority of the runs for the Virtex-5 were done at 6.25 and 12.5MHz with only a few runs being done at 25MHz. These events are due to direct upsets of the DSP registers, or to inadvertent latching of SETs on the data and control lines of the register, or to SETs on the clock lines that result in only a single clock cycle being corrupted.

3) T-duration > 1 Clock-Cycle to T-duration < 50 Microseconds Events

The events in this time regime were not expected prior to these experimental campaigns. They were measured in all dynamic tests, at each facility, with all DUT devices and DUT PCBs tested, at every frequency exercised, and in both the Virtex-4 and Virtex-5 devices. They are particularly obvious in the Virtex-5 measurements, where thousands of these events were captured. While for the Virtex-4, the non-RHBD configuration cell sensitivity effectively masks functional plane SEUs from being captured as often. These unexpected SEE manifestations are defined by a time-signature that is repeatable and consistent within a range of several hundred nanoseconds to about 10 microseconds, centering around 1 microsecond for the Virtex-5, and around 2 microseconds for the Virtex-4. These events demonstrate a slightly reduced cross-section when compared to the single clock-cycle duration events, as is shown in the 3-dimensional plots in Fig. 11. Fig. 6 plots the average duration of this unique SEE manifestation vs. LET for the Virtex-5 measurements, where they appear to be independent of test frequency, and increase slightly with increasing LET.

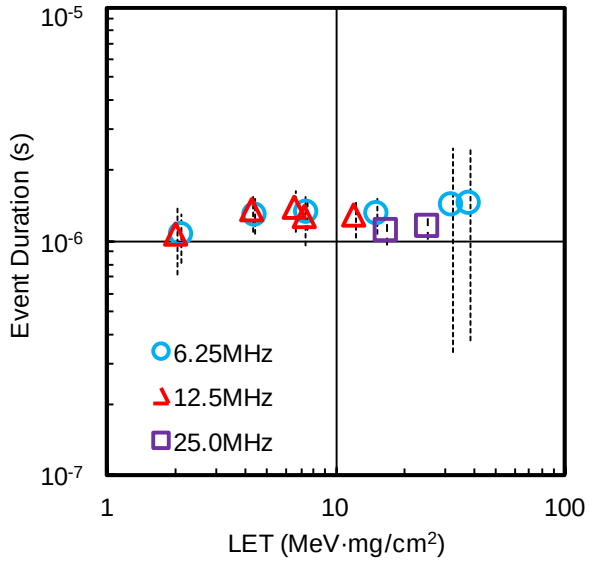

Fig. 6. Regime 3 SEEs vs. LET for the Virtex-5 measurements.

C. Events affecting Multiple DSPs Simultaneously

Events were measured that were observed to simultaneously affect more than one DSP cell at the same exact time. The test system allowed to capture the precise time of occurrence for each SEU observed, within a 10 nanosecond resolution. These events are highlighted with a dark 'X' on top of the event circle marker in Fig. 10 (a) and (b). Many of these events affecting multiple DSPs were captured when the DUT device was reconfigured by the configuration monitoring system upon SEFI detection, as was expected. However, a certain number of repeatable simultaneous events, which we will refer to as a Multiple DSP Upsets (MDU), were observed in duration regimes 2 and 3, which was unexpected. The MDUs were believed to be due to the shared aspects of the three DSPs being monitored, which for the dynamic test DUT design were the clock and the input user control and operators, as shown in Fig. 3. Even though this multiple-DSP upset signature was unexpected, the apparent low-rate of occurrence, manifesting only in less than 1% of all events observed, deemed them not very worrisome from a FPGA user perspective.

To verify the impact of MDUs to a DSP FPGA design, a TMR'd DSP DUT design was developed and irradiated. The

TMR design implemented a common clock, and common operator and control signals to the three voting legs of the TMR design in the same fashion as the single string DSP test design. These single points of failure (SPF) were not expected to disrupt the TMR-voting, since in the non-TMR dynamic tests the MDUs resulted in an insignificant impact to the functionality. However, after irradiating the TMR design, this was observed to not be the case and each TMR'd DSP test structure showed an upset rate that was almost as much as the non-TMR'd designs, which was completely unexpected. The cross-section vs. LET plots for the multiplication dynamic TMR experiments is shown in Fig. 7, which also plots the Weibull approximations of the non-TMR'd multiplication experiments. Several different iterations of the TMR design were attempted at different test dates, with essentially the same results; these cross-sections are also indicated in Fig. 7.

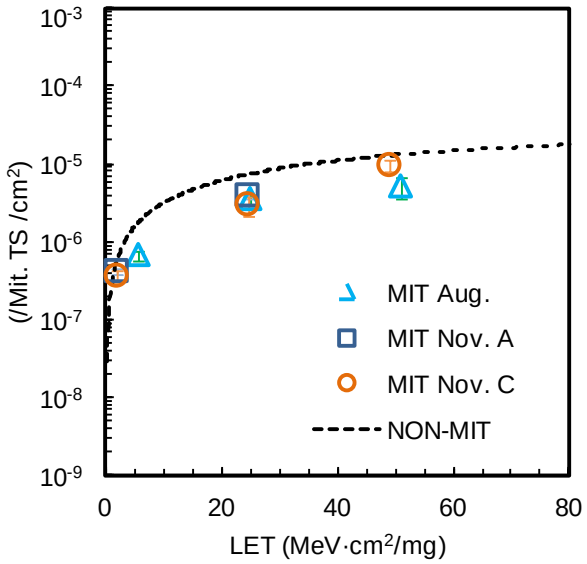

Fig. 7. TMR DSP Test Structure (TS) Cross-section vs. LET for Multiplication operation.

V. Conclusions

Several conclusions can be drawn from the results of these experiments. For the DSPs embedded in the Virtex-5 FPGAs, as is shown in Table III, direct register upsets are shown to make up a significant contribution to the overall sensitivity of the DSP cells, with the other main contributor being attributed to clock tree SETs. We arrive to this conclusion because with the relatively low frequencies employed during the test, very few inadvertent captures of SETs on data and control inputs were expected. Support for this conclusion may be found in the CLB SET-filter testing done by other members of the XRTC, which demonstrate that clock tree SETs dominate the upset rates at frequencies below 200MHz. This is shown in Fig. 8, where checker-board pattern test data, which is clock SET sensitive, is not susceptible to increases in frequency until frequencies of 200MHz are reached, while non-sensitive data patterns are sensitive to increasing frequency. This demonstrates that SETs present at the data and control inputs of the CLB registers do not become an issue until higher frequencies are used [17].

For the DSPs embedded in the Virtex-4, since they do not posses RHBD configuration cells, it was shown here that the SEE susceptibility of the configuration plane greatly overshadows the SEE susceptibility of the functional plane. The Virtex-4 DSPs functional plane could very well have the same susceptibility issues as the Virtex-5 DSPs, but from a user perspective, any conclusions drawn about their functional plane sensitivity are strictly anecdotal since the overwhelming majority of the sensitivity of the Virtex-4 DSP is due to configuration plane upsets.

Another conclusion drawn by these experiments is that the topography of the clock tree employed by the DUT design is a significant factor in the susceptibly of the clock tree to generate SETs. And clock tree SETs have also been observed to simultaneously affect more than one of the nodes that the clock network feeds. This is especially evident in the TMR vs. non-TMR DSP experiments, where simultaneous SEE manifestations that are capable of upsetting the TMR voting mechanisms increase by more than an order of magnitude, as is shown in Fig. 9 DSPs are specially sensitive to this issue since they do not possess the SET filters at the clock input like the Virtex-5 CLB flip-flops do, which filter these SETs as its been shown by the low on-orbit upset rate reported in [17].

From a user perspective, the DSPs available in the Virtex-4 and Virtex-5 devices appear feasible for space applications. The intrinsic nature of the DSPs, which effectively are digital data pipe-line elements, re-loading all registers at every clock-cycle, deems the impact of SEEs as simple noise interference. Further verification is needed to understand the sensitivity of the DSP registers to capturing SETs generated by any upstream combinatorial elements that feed operator and control inputs. This particular SET upset mechanism should be verified at high-frequencies. The embedded DSP space user should also understand the on-orbit upset rate that their DSP application design is susceptible to, and every FPGA design that is intended for space should be analyzed to verify these effects are accounted for.

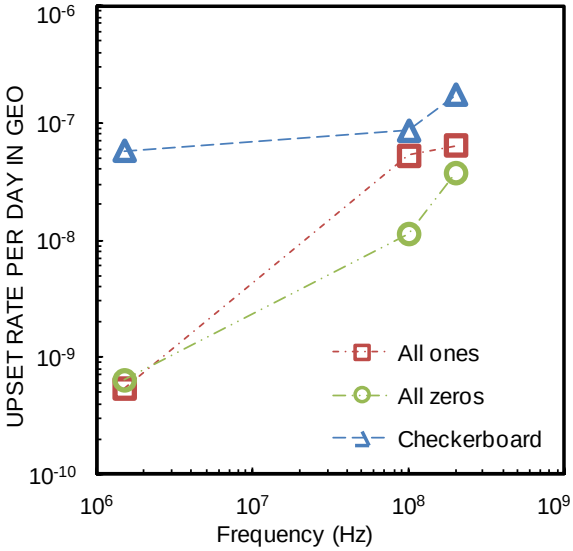

Fig. 8. Virtex-5 CLB-FF upset rate vs. frequency, from [17].

Finally, the method employed in performing SEE experiments by recording both the time and duration of each

SEU has proven to be extremely valuable in exposing key SEE response types that have impact on FPGA designs incorporating DSPs. This SEE testing method was uniquely able to clearly expose these SEE responses and achieve the following:

1. Separation of configuration plane SEUs from functional plane SEUs; demonstrating the major, positive impact of the RHBD configuration cells on the SEE mechanisms of DSPs.
2. Identification of Multiple DSP Upsets events, or MDUs, which affect more than one DSP simultaneously. The MDU susceptibility was also shown to be highly dependent on the topography of the FPGA design's clock tree. This is information is particularly critical for partial or local TMR implementations [18], as well as for generating space FPGA DSP designs to be as least sensitive to SEEs as possible.
3. Identification of a non-frequency dependant DSP SEE manifestation; this manifestation has never been reported by the community prior to this work to the best of the authors knowledge.

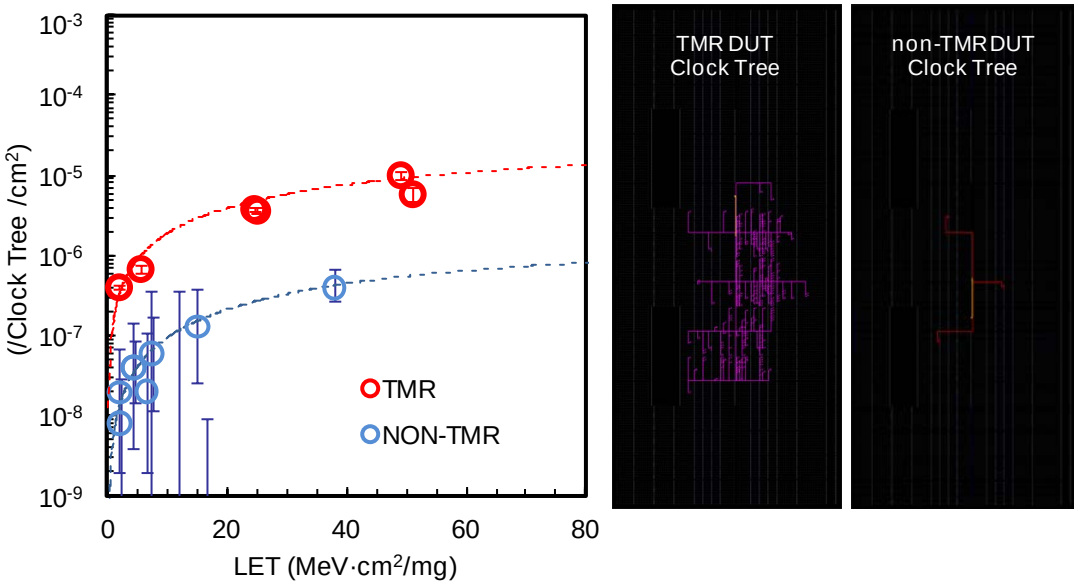

Fig. 9. Cross-Section vs. LET for MDUs of TMR DUT Clock Tree and non-TMR clock Tree, and on the right, the topography of each clock tree.

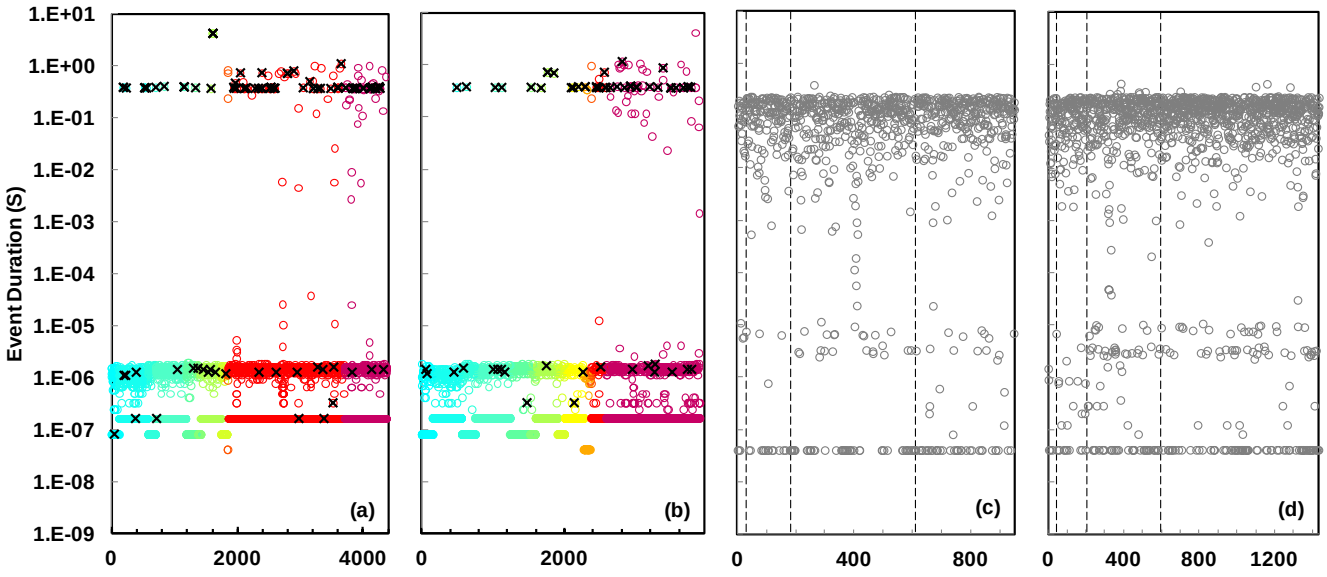

Fig. 10. Event duration charts of DSP SEUs for Virtex-5 Addition (a) and Multiplication (b) operations, and for Virtex-4 Addition (c) and Multiplication (d) operations.

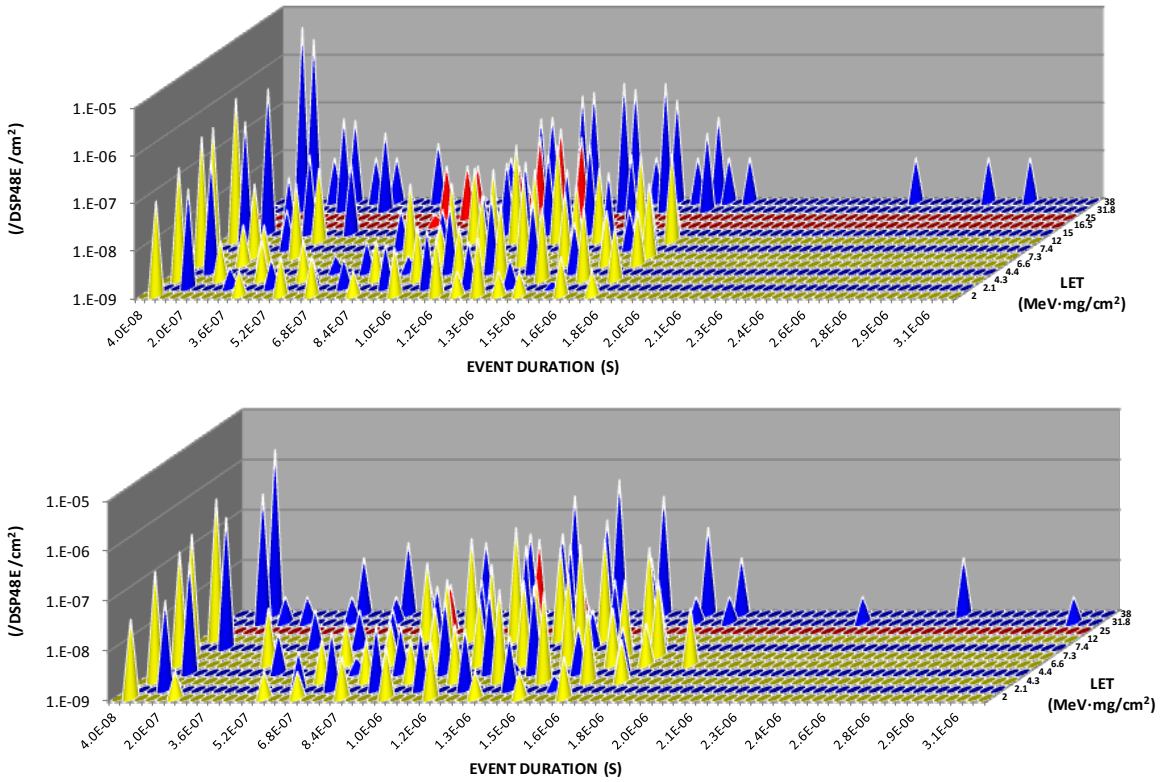

Fig. 11. Event Cross-Section vs. LET vs. Event Duration, in 40ns Bins, Shown for Multiplication (top) and Addition (bottom) operations in the Virtex-5; each cone represents a 40ns event bin, and each color indicates a different test frequency (Blue = 6.25MHz, Yellow = 12.5MHz, and Red = 25MHz).

VI. Acknowledgments

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